Docket No.: M&N-IT-197

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : MARTIN EHLERT ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD AND CONFIGURATION FOR GENERATING A COCK PULSE IN A DATA PROCESSING SYSTEM HAVING A NUMBER OF DATA CHANNELS

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,317,288 (Yung et al.), dated May 31,1994;

U.S. Patent No. 5,614,855 (Lee et al.), dated March 25, 1997;

German Published, Non-Prosecuted Patent Application 198 34 416 A1 (Miyano), dated February 4, 1999, pertains to a clock signal generator;

German Published, Non-Prosecuted Patent Application 198 30 571 A1 (Buck), dated January 13, 2000, pertains to an integrated circuit;

Published European Patent Application No. 0 349 715 A2 (Rein), dated January 10, 1990, pertains to a method and circuit arrangement to produce a out-of-phase clock signal;

Lee, Thomas H. et al.: "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE, Vol. 29, No. 12, December 1994, pp. 1491-1496 and

Kim, C. et al.: "A 640 MB/s Bi-Directional Data Strobed, Double-Data-Rate SDRAM with a 40 mW DLL Circuit for a 256 MB Memory System", IEEE, February 6, 1998;

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

For Applicants

Date: November 30, 2001

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: M&N-IT-197 Applicant MARTIN EHLERT ET AL. Filing Date NOVEMBER 30, 2001

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	5,317,288	5/31/94	Yung et al.			
	B	5,614,855	3/25/97	Lee et al.			
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	19834416A1	02/04/99	Germany				X
	K	19830571A1	01/13/00	Germany				X
	L	0349715A2	01/10/90	Europe				X
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Lee, Thomas H. et al.: "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE, Vol. 29, No. 12, December 1994, pp. 1491-1496
		Kim, C. et al.: "A 640 MB/s Bi-Directional Data Strobed, Double-Data-Rate SDRAM with a 40 mW DLL Circuit for a 256 MB Memory System", IEEE, February 6, 1998

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.